

The Economics of ASICs: At What Point Does a Custom SoC Become Viable?

ASICs aren't the preserve of only the richest in Silicon Valley. EnSilica's Ian Lankshear looks at the economics behind developing an ASIC and how to keep costs to a minimum.

Much has been made in the press recently of the rising use of custom ASICs among Silicon Valley's biggest tech firms. It's part of a drive to create cutting-edge artificial-intelligence chips and cloud-computing services.

In April, it was Tesla reporting its ASICs for self-driving vehicles. In February, it was Facebook. And before those, Amazon and Google. Indeed, Amazon's 2015 acquisition of Annapurna Labs, which gives Amazon the ability to create the ASICs that runs its EC2 software at a higher speed and lower cost, was recently cited by Forbes as "one of the most successful and strategic acquisitions for Amazon, [giving Amazon Web Services] an edge against its arch-rivals, Microsoft and Google."

Amazon purchased Annapurna for \$350 million. And

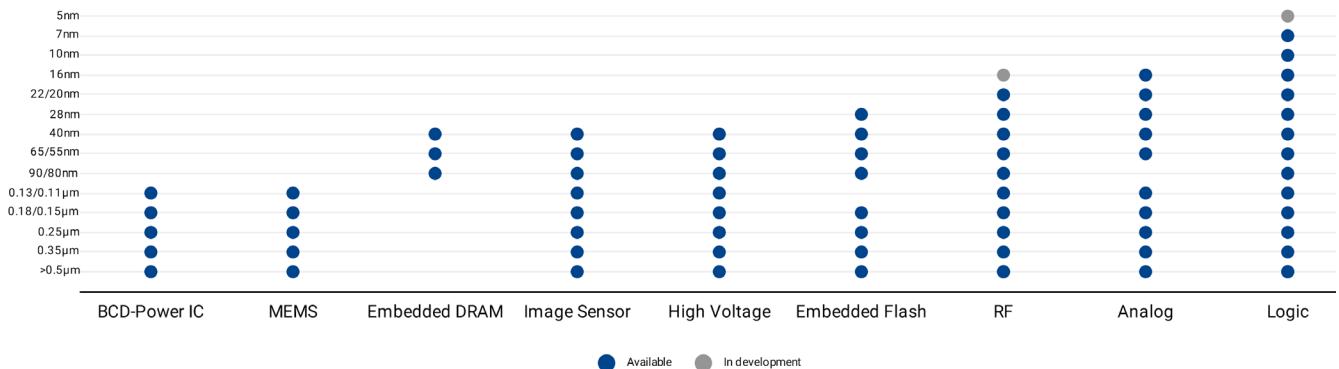
anecdotal mentions of hefty sums for a single mask set (with seven zeros)/design costs that stretch into hundreds of millions of dollars have been reported on for applications that use a leading-edge silicon process technology.

However, these figures are for just that: high-volume, high-value consumer products (such as smartphones) that need the most advanced processes to remain competitive. They're very much not the norm. For many applications, even IoT, taking a custom ASIC route can prove better value than using standard parts. But you need to calculate your ROI carefully, as well as talk to your existing supply chain to make sure a standard part that would solve all your issues isn't on their roadmap.

Here we look at two case studies that outline the costs and break-even point, to ask at what point does a custom ASIC

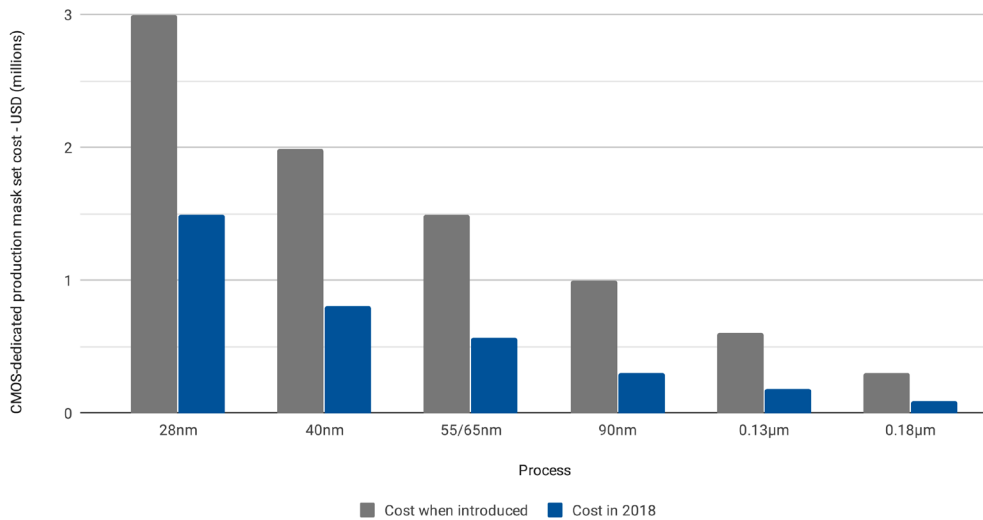
Using 'more than Moore' technologies can significantly cut the cost of an ASIC

TSMC's available processes: May 2019



1. Leading-edge and "more than Moore" processes available from TSMC.

Using mature technologies cuts the mask set costs significantly: 2018 vs cost when each technology was introduced



2. Cost of a CMOS-dedicated production mask for 0.18 µm to 28 nm for 2018 versus when the technology was introduced.

become viable? And what should you know when specifying one?

Economic Trends—Using a More than Moore Approach

The above examples looked at applications that require the most advanced technologies and are at the leading edge of Moore’s Law. For TSMC, this equates to 7-nm processes for logic (with 5 nm due this year) and 22 nm for RF. At these lithographies, mask costs could make your ROI calculation go the wrong way.

However, for real-world applications such as IoT or automotive systems—where power consumption, wireless communications standards, or incorporation of a MEMS sensor are far more important than processing speed—mature “more than Moore” CMOS technology nodes enable a much more cost-effective SoC design to be implemented (Fig. 1).

To put this into context, the cost of a CMOS-dedicated production mask set is in the region of \$1.5 million at 28 nm, \$0.8 million at 40 nm, \$0.5 million at 55/65 nm, and going down to sub-\$100k for 180 nm (Fig. 2). And these values continue to reduce as processes become more mature. A 28-nm mask set is half the cost now versus when it was first introduced, and on the same basis, a 55/65-nm mask set is roughly a third the cost.

The mask set represents a relatively small part of the total ASIC NRE—the IP licensing cost, development and qualification costs can be several times (up to the low tens of times) the mask set NRE. But, by using the mature “more than Moore” technologies, system developers can more affordably create smaller devices that are hard to copy, incorporate more features, and run more efficiently.

When Does it Become Viable to Design an ASIC?

Of course, the process isn’t the only cost implication in designing an ASIC. And, as we’ve already touched on, cost alone isn’t (and shouldn’t be) the only reason to choose an ASIC over off-the-shelf components. But budgets do need to be balanced.

As a reasonable rule of thumb, you should consider an ASIC over off-the-shelf components if:

- You’re looking to achieve a design that’s smaller, more efficient, and harder to imitate.
- Electronic component spend per product line exceeds \$2M.

So here we look at two examples that outline the cost of an ASIC versus standard components—for existing systems (where sales figures are already known) and for new products.

Both are anonymized real-world examples from late 2016. They show the approximate cost of developing the ASIC and the point at which they become more cost-effective than off-the-shelf components.

Example 1: Replacing the MCU and analog components in an automotive system

As part of an automotive system, EnSilica was asked to replace the MCU (cost \$2.80* per unit) and multiple discrete analog components (total cost \$2.69 per unit) with an automotive-qualified ASIC. This would run alongside a CAN/LIN transceiver, an accelerometer, and the PCB/sundries (Fig. 3).

The system developer shipped between 40-45,000 units per month, and NRE development costs for the ASIC design and mask set were \$1M (for the 130-nm ASIC with flash, analog metals, and thick oxide), plus the automotive qualification

AEC-Q100/productization costs of \$392,000. The ASIC unit price was \$1.46.

Based on its lower value of 40,000 units, the return on investment is reached in less than nine months, with a 12X return on investment after a mask life of nine years (Fig. 4). And even if their sales dropped by half, this would change to <18 months and 6X return on investment after nine years.

Example 2: Creating an ASIC for a new medical IoT telemetry system

As per the above, cost alone isn't the only reason to take an ASIC approach. Often, the power consumption of, or the feature set included in, off-the-shelf components doesn't meet the demands of the system.

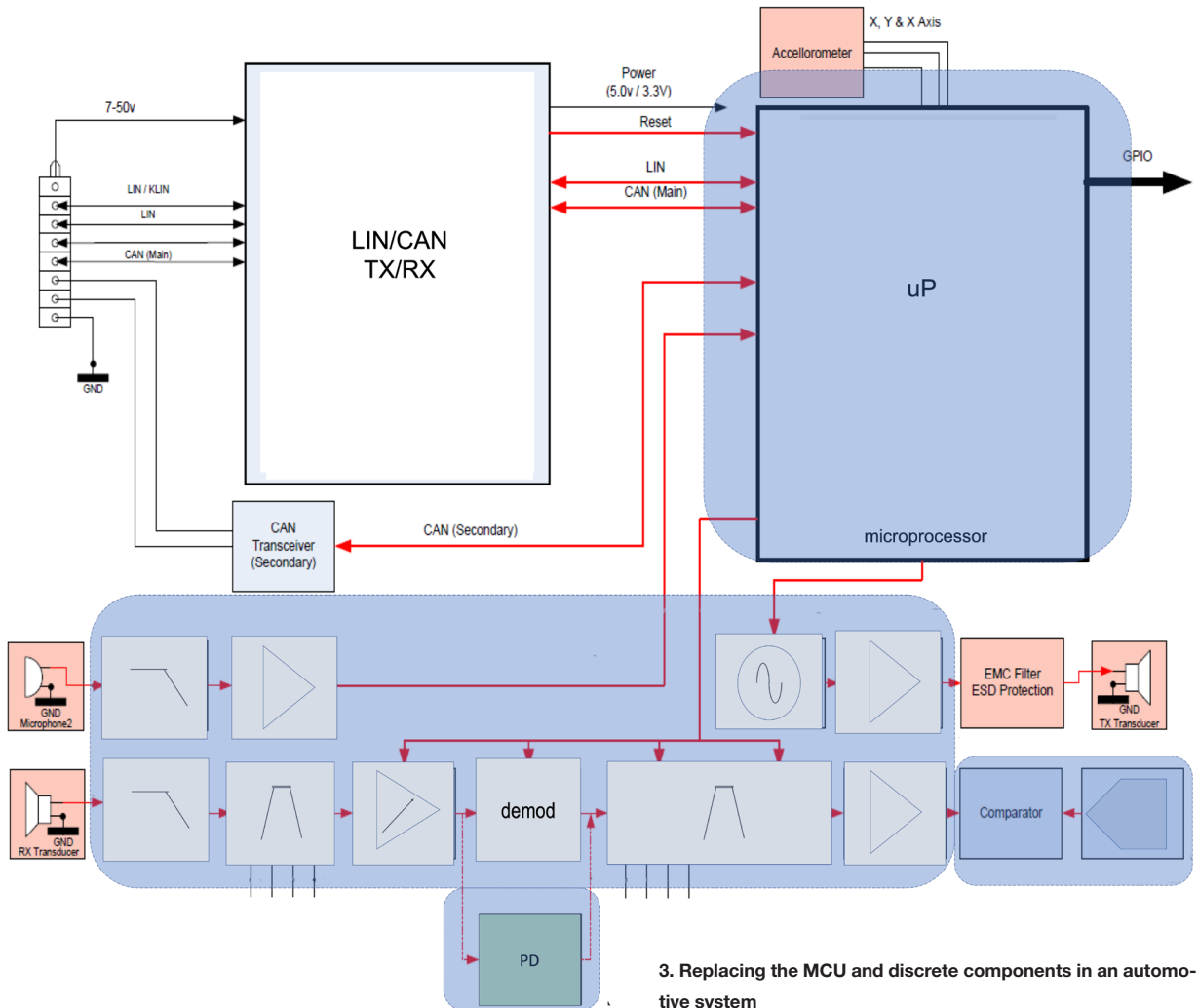
For this example, we look at a medical device company that approached EnSilica when developing a new healthcare IoT system to continuously monitor ECG, heart rate, respiration rate, and temperature monitoring (Fig. 5). It would transmit this data (>50 m) back to the server for real-time monitoring

and use a small battery to power the system continuously for at least five days. And it must do so in a way that would not prevent FDA 510k (U.S. medical device safety certification) approval.

The ASIC would therefore need to integrate a sensor interface, low-power wireless-standard (in this case Bluetooth LE) wireless transceiver, power management, microprocessor, and flash memory using a 65-nm process, where low power was vital to the product's success.

Cost was still a significant factor in the decision, though, with the wearable device needing to be a single-use system to prevent any spread of diseases, and to be priced accordingly. Not only would the power consumption of off-the-shelf components fallen outside the allowable power budget, discrete components would have had a combined cost \$7.56 per unit, versus NRE costs of \$5.3 million and a unit price of \$2.30 for the ASIC.

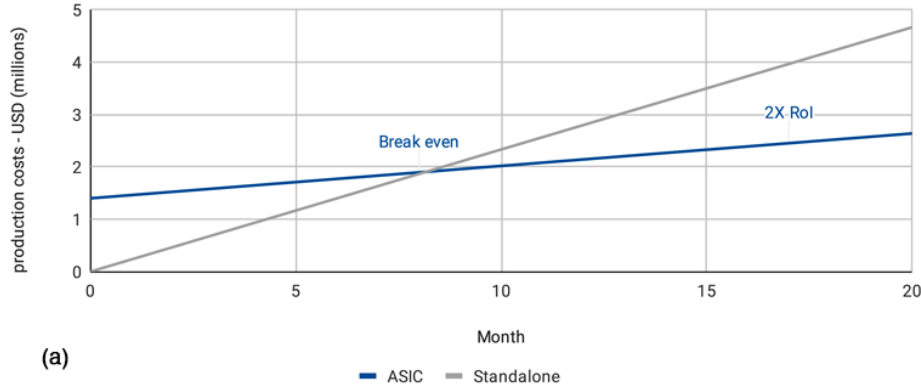
Based on these figures, the OEM would need to ship 1 million units to break even versus an off-the-shelf route.



3. Replacing the MCU and discrete components in an automotive system

Replacing μ P and analog components in an automotive ASIC using a 130nm process achieved RoI in less than 9 months

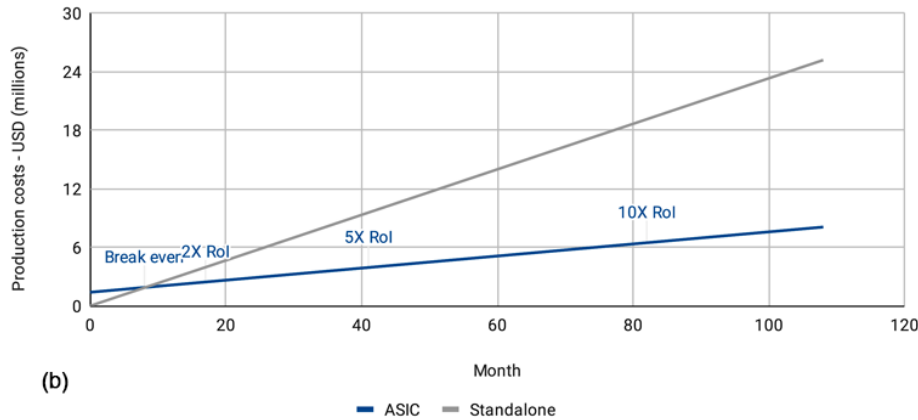
Based on \$1.4m NRE costs, \$4.03 unit saving, shipping 40,000 units per month



4. ROI is seen in less than nine months (a). A 13.2X ROI is seen after the systems' nine-year production life (b).

And saw a lifetime RoI of 13.2X

Based on a 9-year lifespan



Developing an ASIC using a 65nm process cut power demands and cost for a disposable patient monitoring device - with RoI after 1 million units

Based on £5.3m NRE costs, \$5.26 unit saving



5. ASIC or off-the-shelf components—the economics behind the choice for a healthcare monitoring IoT system.

Conversely, using off-the-shelf components would have meant both the high power and the high unit cost would have killed the product.

Caption:

Conclusion (and Considerations to Improve Your ROI)

As the above examples show, developing a custom ASIC is no longer the preserve of Silicon Valley's biggest firm—and even for (in fact, especially for) IoT devices where devices often need to be simple, small, low power, and often low cost. An ASIC approach will often be the most cost-effective option and makes it easier as manufacturing scales up.

Whether you're designing in-house or using a custom ASIC developer, there are three golden rules you can use to keep NRE costs lower and increase your RoI.

1. *Measure twice, cut once:* A simple remote IoT sensor has different requirements to a smart appliance. It's crucial to understand exactly what is available in the market, and what unique functionality/user experience customers expect/would like? A good specification is crucial to success, to borrow a phrase from the building trade: measure twice, cut once. Plan everything well. The alternative will be a custom ASIC that's missing features, or one that's over-specified. Both ways, the advantages over standard parts is lost.

2. *Don't reinvent the wheel:* Just as using mature processes will significantly cut mask-set costs, using proven IP blocks (such as those from Arm) enables you to design a custom SoC much more quickly. And it significantly reduces the risk of not getting it right first-time.

3. *Reuse your software:* Software development significantly impacts both project NRE and time-to-market. Indeed, the development of tools and software are probably the biggest investment you will make for the project. Therefore, reusing existing applications and software libraries can greatly help control project cost and accelerate the time-to-market.

Factor this into the ASIC design and ensure that future designs (be they based on a new ASIC or off-the-shelf hardware) are able to reuse and build upon your existing software.

One way to do this is through the use of licensable IP—it will massively reduce the risk and time to market. For example, the Arm Cortex-M0 and Cortex-M3 processors are available at zero license fee through the company's DesignStart program. Similarly, licensable IP is available from many vendors for standard peripherals such as I²C and SPI, interfaces for USB, PCIe controllers, and PHYs; and wireless including Bluetooth LE and Wi-Fi.

Ian Lankshear is the managing director and co-founder of EnSilica, a leading fabless design house focused on custom ASIC design as well as supply and design services. The company has extensive expertise in designing and supplying custom analog, mixed-signal, and digital ICs to its customers worldwide in the automotive, industrial, and consumer markets.